What is Claimed is:

1. A parallel signal automatic phase adjusting circuit having a number of data signal channels inputted together with a clock signal and adjusting the clock signal so that the clock signal is synchronized with each of the data signals, the parallel signal automatic phase adjusting circuit comprising:

a signal generator for generating a signal having a predetermined frequency smaller than a frequency which is utilized as the data signal or the clock signal;

an oscillating circuit for generating a clock signal having a frequency smaller than the inputted clock signal by the predetermined frequency generated from the signal generator; and

adjusting circuits provided in correspondence to the respective data signal channels for effecting adjustment on the clock signal generated from the oscillating circuit so that the clock signal is synchronized with the corresponding data signal, based on an arithmetic operation of trigonometric functions using phase comparing information deriving from comparison between each of the data signal and the clock signal generated from the oscillating circuit and frequency information regarding the respective data signals, the clock signal generated from the oscillating circuit and the signal supplied from the signal generator.

2. A parallel signal automatic phase adjusting circuit having a number of data signal channels inputted together with a clock

signal and adjusting the clock signal so that the clock signal is synchronized with each of the data signals, the parallel signal automatic phase adjusting circuit comprising:

an oscillating circuit for generating a clock signal having a frequency smaller than the inputted clock signal by a predetermined frequency; and

adjusting circuits provided in correspondence to the respective data signal channels for effecting adjustment on the clock signal generated from the oscillating circuit so that the clock signal is synchronized with the corresponding data signal, based on an arithmetic operation of trigonometric functions using as a parameter, phase comparing information deriving from comparison between each of the data signal and the clock signal generated from the oscillating circuit, frequency information regarding the clock signal and the data signals, and the frequency information of the predetermined frequency.

3. A parallel signal automatic phase adjusting circuit having a number of data signal channels inputted together with a clock signal and adjusting the clock signal so that each clock signal is synchronized with each of the data signals, the parallel signal automatic phase adjusting circuit comprising:

adjusting circuits provided in correspondence to the respective data signal channels for effecting adjustment on the clock signal generated from the oscillating circuit so that the clock signal is synchronized with the corresponding data signal: wherein

each of the adjusting circuits is arranged to include a phase comparator for comparing the clock signal and the data signal in phase, and

a trigonometric function calculating unit for effecting adjustment on the clock signal so that the clock signal is synchronized with the data signal, based on trigonometric function calculation using phase comparing information supplied from the phase comparator as a parameter.

4. A parallel signal automatic phase adjusting circuit according to Claim 1, wherein

each of the adjusting circuit is arranged to include a phase comparing delay circuit which is supplied with a signal from the signal generator, compares the corresponding data signal with the clock signal as a target of adjustment and generates phase comparing information therefrom as a result of comparison together with frequency information of a signal from the signal generator, and

a calculating circuit for effecting adjustment on the clock signal generated from the oscillating circuit so that the clock signal is synchronized with the corresponding data signal based on the trigonometric function calculation using the clock signal supplied from the oscillating circuit and the information supplied from the phase comparing delay circuit.

5. A parallel signal automatic phase adjusting circuit according to Claim 2, wherein

each of the adjusting circuit is arranged to include a

phase comparing oscillating circuit which oscillates at a frequency identical to the predetermined frequency (decreased by the oscillating circuit), compares the corresponding data signal with the clock signal as a target of adjustment, and generates phase difference information therefrom as the frequency information, and

a calculating circuit for effecting adjustment on the clock signal generated from the oscillating circuit so that the clock signal is synchronized with the corresponding data signal based on the trigonometric function calculation using the clock signal supplied from the oscillating circuit and the information supplied from the phase comparing delay circuit as parameters.

6. A parallel signal automatic phase adjusting circuit according to Claim 1, comprising an inter-data phase adjusting circuit which is supplied with the clock signals having undergone adjustment by the respective adjusting circuits together with the corresponding data signal, and generates a plurality of kinds of data in synchronism with the timing of the most delayed clock signal

7. A parallel signal automatic phase adjusting circuit according to Claim 2, comprising an inter-data phase adjusting circuit which is supplied with the clock signals having undergone adjustment by the respective adjusting circuits together with the corresponding data signal, and generates a plurality of kinds of data in synchronism with the timing of the most delayed clock

signal.

8. A parallel signal automatic phase adjusting circuit according to Claim 3, comprising an inter-data phase adjusting circuit which is supplied with the clock signals having undergone adjustment by the respective adjusting circuits together with the corresponding data signal, and generates a plurality of kinds of data in synchronism with the timing of the most delayed clock signal.

9. A parallel signal automatic phase adjusting circuit according to Claim 6, wherein the inter-data phase adjusting circuit is arranged to include a clock selecting circuit for selecting a clock signal having the most delayed timing from clock signals having undergone adjustment in the respective adjusting circuits, and

a data output section for generating at the same timing data signals other than the data signal corresponding to the clock signal selected by the clock selecting circuit, based on the clock signal selected by the clock selecting circuit.

10. A parallel signal automatic phase adjusting circuit according to Claim 7, wherein the inter-data phase adjusting circuit is arranged to include a clock selecting circuit for selecting a clock signal having the most delayed timing from clock signals having undergone adjustment in the respective adjusting circuits, and

a data output section for generating at the same timing

data signals other than the data signal corresponding to the clock signal selected by the clock selecting circuit, based on the clock signal selected by the clock selecting circuit.

11. A parallel signal automatic phase adjusting circuit according to Claim 8, wherein the inter-data phase adjusting circuit is arranged to include a clock selecting circuit for selecting a clock signal having the most delayed timing from clock signals having undergone adjustment in the respective adjusting circuits, and

a data output section for generating at the same timing data signals other than the data signal corresponding to the clock signal selected by the clock selecting circuit, based on the clock signal selected by the clock selecting circuit.

12. A parallel signal automatic phase adjusting circuit according to Claim 9, wherein the data output section is composed of a number of data output units provided so as to correspond to the data signal channels, respectively, each of the data output units being made up of a flip-flop circuit operable in response to the selected clock signal.

13. A parallel signal automatic phase adjusting circuit according to Claim 10, wherein the data output section is composed of a number of data output units provided so as to correspond to the data signal channels, respectively, each of the data output units being made up of a flip-flop circuit operable in response to the selected clock signal.

14. A parallel signal automatic phase adjusting circuit according to Claim 11, wherein the data output section is composed of a number of data output units provided so as to correspond to the data signal channels, respectively, each of the data output units being made up of a flip-flop circuit operable in response to the selected clock signal.

15. A parallel signal automatic phase adjusting circuit according to Claim 6, wherein the inter-data phase adjusting circuit is arranged to include a clock selecting circuit for selecting a clock signal having the most delayed timing from clock signals having undergone adjustment in the respective adjusting circuits, and for generating a data signal corresponding to the selected clock signal,

a data output section for generating all of the data signals at the same timing based on the clock signal selected by the clock selecting circuit, and

a register circuit section capable of compensating for a phase deviation exceeding one time slot amount based on bit information of respective data signals.

16. A parallel signal automatic phase adjusting circuit according to Claim 7, wherein the inter-data phase adjusting circuit is arranged to include a clock selecting circuit for selecting a clock signal having the most delayed timing from clock signals having undergone adjustment in the respective adjusting circuits, and for generating a data signal

corresponding to the selected clock signal,

a data output section for generating all of the data signals at the same timing based on the clock signal selected by the clock selecting circuit, and

a register circuit section capable of compensating for a phase deviation exceeding one time slot amount based on bit information of respective data signals.

17. A parallel signal automatic phase adjusting circuit according to Claim 8, wherein the inter-data phase adjusting circuit is arranged to include a clock selecting circuit for selecting a clock signal having the most delayed timing from clock signals having undergone adjustment in the respective adjusting circuits, and for generating a data signal corresponding to the selected clock signal,

a data output section for generating all of the data signals at the same timing based on the clock signal selected by the clock selecting circuit, and

a register circuit section capable of compensating for a phase deviation exceeding one time slot amount based on bit information of respective data signals.

18. A parallel signal automatic phase adjusting circuit according to Claim 15, wherein the register circuit section is arranged to include a plurality of shift registers connected in a cascade fashion so as to correspond to respective data signal channels, each of the shift registers being capable of holding data of corresponding data signal channel, and

selectors provided so as to correspond to respective data signal channels so that each selector is supplied with an output signal from the shift registers in the corresponding data signal channel, all of the selectors being capable of outputting respective data stream at the same timing in response to a select signal useful for extracting data pieces having the same timing.

19. A parallel signal automatic phase adjusting circuit according to Claim 16, wherein the register circuit section is arranged to include a plurality of shift registers connected in a cascade fashion so as to correspond to respective data signal channels, each of the shift registers being capable of holding data of corresponding data signal channel, and

selectors provided so as to correspond to respective data signal channels so that each selector is supplied with an output signal from the shift registers in the corresponding data signal channel, all of the selectors being capable of outputting respective data stream at the same timing in response to a select signal useful for extracting data pieces having the same timing.

20. A parallel signal automatic phase adjusting circuit according to Claim 17, wherein the register circuit section is arranged to include a plurality of shift registers connected in a cascade fashion so as to correspond to respective data signal channels, each of the shift registers being capable of holding data of corresponding data signal channel, and

selectors provided so as to correspond to respective data signal channels so that each selector is supplied with an output

signal from the shift registers in the corresponding data signal channel, all of the selectors being capable of outputting respective data stream at the same timing in response to a select signal useful for extracting data pieces having the same timing.

21. A parallel signal automatic phase adjusting circuit according to Claims 1, wherein each of the adjusting circuits is arranged to include a temperature sensor for compensating for the temperature dependability of the phase comparing information.

22. A parallel signal automatic phase adjusting circuit according to Claims 2, wherein each of the adjusting circuits is arranged to include a temperature sensor for compensating for the temperature dependability of the phase comparing information.

23. A parallel signal automatic phase adjusting circuit according to Claims 3, wherein each of the adjusting circuits is arranged to include a temperature sensor for compensating for the temperature dependability of the phase comparing information.